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ASMEX.320A

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Pomarede, et al.	) Group Art Unit Unknown
Appl. No.	:	10/074,722	)
Filed	:	February 11, 2002	)
For	:	INTEGRATION OF HIGH K GATE DIELECTRIC	)
Examiner	:	Unknown	)

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: United States Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202, on

4/9/02
(Date)

Joseph J. Mallon
Joseph J. Mallon, Reg. No. 39,287

PRELIMINARY AMENDMENT

United States Patent and Trademark Office
P.O. Box 2327
Arlington, VA 22202

Dear Sir:

Prior to examination, please amend the above-referenced application as follows:

IN THE ABSTRACT:

Please replace the Abstract of the Disclosure with the following new Abstract:

Methods are provided herein for forming electrode layers over high dielectric constant ("high k") materials. In the illustrated embodiments, a high k gate dielectric, such as zirconium oxide, is protected from reduction during a subsequent deposition of silicon-containing gate electrode. In particular, a seed deposition phase includes conditions designed for minimizing hydrogen reduction of the gate dielectric, including low hydrogen content, low temperatures and/or low partial pressures of the silicon source gas. Conditions are preferably changed for higher deposition rates and deposition continues in a bulk phase. Desirably, though, hydrogen diffusion is still minimized by controlling the above-noted parameters. In one embodiment, high k dielectric reduction is minimized through omission of a hydrogen carrier gas. In another embodiment, higher order silanes aid in reducing hydrogen content for a given deposition rate.